REMARKS

Reconsideration of the application is requested.

Claims 1-20 remain in the application. Claims 1-20 are subject to examination. Claims 1-4 and 20 have been amended.

Under the heading "Specification" on page 2 of the above-identified Office Action, the Examiner objected to the specification because of two (2) informalities on pages 14 and 15. The Examiner's suggested corrections have been made where "L1" has been changed to "L2".

Under the heading "Claim Rejections - 35 USC § 112" on pages 2-3 of the above-identified Office Action, claims 1-20 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that the latch stage and the latch device are the same thing and therefore the claim is misdescriptive. Applicant respectfully disagrees and believes that each of the latch stages contains an input terminal 8, an output terminal 9 and the latch device 6 with the multiplexer 7 disposed between the input and output terminal 8, 9. Applicant believes that this is an abstract combination and respectfully requests the Examiner to

reconsider the rejection. Please note that claim 1 was amended to recite the input terminal.

The Examiner further states that lines 12-13 are misdescriptive in that the data provided to the output terminal is stored in the preceding stage and not in the latch device as described.

The Examiner is correct in that the respectively existing preceding latch stage Lj-1 of a subsequent latch stage Lj provides the data buffered therein as the input data. However, after receiving the data provided by the preceding latch stage Lj-1, the data are received by the following latch stage Lj and are there buffered by the following latch stage Lj, which creates a corresponding delay time or latency. This is the object of the invention and is realized by the feedback loops 20 and 21. In summary, the output data D_{out} which is provided by the respective latch stage Lj and in particular by the first latch stage L1 at the data output terminal 9 are data which are buffered only indirectly, i.e. indirectly by the preceding latch stage Lj-1. In an immediate or direct manner, however, the data is further buffered by the latch stage in question Lj or by the first latch stage L1 itself.

In order to emphasize this matter more strongly, claim 1 has been amended with the phrase "either….or" with reference to the first and second selection state of the multiplexer.

The Examiner further objects to the phrase "can be" in line 23. This phrase has been changed to "are" to overcome the rejection. Similar changes were made to claims 2, 3 and 20.

Claim 4 was amended to correspond to the change made in claim 1.

Because of the above-mentioned explanation and/or changes the objections to claims 12-19 are also believed to be overcome.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In view of the foregoing, reconsideration and allowance of claims 1-20 are solicited.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicant

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REL:cgm

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